Finite Element Modeling of System Design and Testing Conditions for Component Solder Ball Reliability Under Impact

Xuejun Fan and Amarinder Singh Ranouta

***Abstract*— In this paper, the effects of system design and testing conditions on the dynamic behavior of solder balls of components are studied through finite element analysis. The current JEDEC drop test board (JESD22-B111) is used as a baseline model. The model is then extended to several new configurations, which consider the effects of major component placement, secondary component attachment, and drop orientations at system level. Some findings are summarized as follows. There exists a region near the mounting support, where the board bends in the opposite direction as the board in the center. This localized bend mode causes excessive stresses in solder balls for the components close to the mounting support areas. The attachment of a secondary component on the opposite side of a major component has different effects: symmetric placement can reduce the stresses in the major component. However, the off-centered placement gives rise to the additional stresses in solder balls on the far edge of the major component, and therefore can lead to a higher failure rate. Components respond differently under 0° (face-down) and 180° (face-up) horizontal drops, respectively, as the magnitude of tensile and compressive stresses in one vibrational period is not symmetric. In addition, horizontal drop may be the worst drop orientation for solder ball damages, compared to the other drop orientations. The vertical (90°) drop has very limited damages to solder balls. The above findings and predictions have been verified experimentally. The results provide insight to the system- and board-level designs in product development.**

***Index Terms*— Drop test, finite element analysis (FEA), impact, reliability, solder ball, system design.**

I. Introduction

DROP TEST performance has been one of the key package reliability indicators for portable applications. A board-level drop test standard, JESD22-B111, has been published by the Joint Electronic Device Engineering Council (JEDEC) for the components used in handheld electronic products [1]. This allows the evaluation of component (or package) performance under a fixed board and testing condition. There have been numerous studies at component level on the effects of structure, material, and geometry of components [2]–[10]. Component performance at board and system levels, however, becomes even more complicated, since there are many additional factors: the size and thickness of printed circuit board (PCB), major component locations, the placement of secondary components (either on the same or opposite side of PCB), and the enclosure design are the examples of these factors at board and system levels. In addition, during real-life drops, a device may experience different impact orientations. Not only the magnitude of dynamic stress/strain but also the dominant stress/strain component in solder balls is affected by the impact orientation [5], [11].

Owing to the lack of experimental methods/tools for measuring stress/strain of solder balls, finite element modeling has been employed to study the failure mechanism of solder balls under drops. The so-called input-G method, in which the board-level model is analyzed using the drop table acceleration as input loading, decouples the board finite element model from the system model [12]. There are several approaches in implementing the input-G method. Tee *et al.* [3] used explicit dynamics analysis by directly applying acceleration impulse using DYNA-3-D. Syed *et al.* [6] introduced the large mass method to convert acceleration input into force input by multiplying the acceleration with a large mass with implicit dynamics. Irving *et al.* [13] proposed the input-D method, in which the acceleration input is integrated twice to obtain the displacement boundary condition over time. Loh *et al.* [14] used mode superposition method for a linear system under impact loading. Shen *et al.* [15] and the authors of [7]–[10], [16], and [17] introduced the direct acceleration input method as an alternative to apply the impulse loading while removing the rigid body motion. In this method, the acceleration impulse is applied as body forces to the problem under study. To reduce the size of finite element model in terms of CPU usage, several special treatments, such as equivalent layer models for solder interconnects [16], shell element in global models [6], solid-to-solid submodeling technique using half PCB board [7], [16], shell-to-solid submodeling using beam-shell-based quarter-symmetry models [17]–[21], and shell-to-solid submodeling without any assumption of symmetry [22], have been developed. The accuracy of the local modeling (or submodeling) technique has been verified by the comparison of board strain calculations from both global and local models [16].

In this paper, the effects of system design and testing conditions on the dynamic behavior of solder balls of components are studied through finite element analysis. The current JEDEC drop test board model is extended to several new configurations. Wafer-level packages (WLPs) (copper post structure) with different sizes are applied. The effects of major component placement on the board are studied first,

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The authors are with the Department of Mechanical Engineering, Lamar University, Beaumont, TX 77710 USA (e-mail: xuejun.fan@lamar.edu; amarinder.s.me@gmail.com).

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by changing the distance between the corner components and mounting support locations. Then the effect of secondary components attachment is investigated. Three scenarios to consider the effects of both relative position and size of the secondary components are simulated. Finally, the effects of drop orientation are analyzed. Component face-down (0°) and face-up (180°) in horizontal drops, as well as vertical drop (90°) are investigated.

II. Board Configurations and Testing Conditions

In this paper, the JESD22-B111 drop test board is used as a baseline model. This model is extended to several new configurations to investigate the effects of board- and system-level designs and testing conditions.

A. Major Component Placement

According to JESD22-B111, a 132 mm × 77 mm × 1 mm eight-layer PCB is used, and 15 components are mounted on the board, in 3 rows of 5 components, as illustrated in Fig. 1. Based on the symmetry, the 15 components, which are uniquely labeled from U1 to U15, are classified into five groups (Groups A to E). They have distinct failure rates due to the difference in locations. All components must be located within the 95 mm × 61 mm area, and the outer edges of the components (U1 through U6 and U10 through U15) shall align with the boundary of this area. The locations of four mounting screws are specified at a distance of 5 mm in both x- and y-directions from the edge of corner components (Group A: U1, U5, U11, and U15), regardless of component size. Mounting screws not only provide the support for the test board but also serve to transmit the impact energy from system to board.

In this paper, the effect of the distance from corner component to the mounting screws is studied. To keep the fundamental frequencies of the system consistent with the original JEDEC drop test board, the dimensions of the board and the spans between the mounting holes in x- and y-directions remain the same when screw distance from the corner components changes. Fig. 2 shows the geometry of the quarter part of the modified JEDEC board. With screw distance ($D1$) changing, the distances between two consecutive components (labeled as A and B) change accordingly.

B. Placement of Secondary Components

Often secondary components are assembled to the system board in the proximity of a major component on the opposite side of PCB. In this paper, three scenarios are defined to study the effects of both the size and location of the secondary components. Fig. 3 shows the front view of the three scenarios. In scenarios 1 and 2, the secondary components are aligned in the center beneath each major component. The size of the secondary component is smaller than the major one in scenario 1, but greater in scenario 2. Since the component placement is symmetric for both cases, only half the models are shown in Fig. 3(a) and (b). For scenario 3, a large secondary component is placed off-centered with respect to the major component. In this case, the model is not symmetric, and therefore the full model should be used. We will investigate the solder ball stresses in these three scenarios compared to that without the placement of any secondary components.

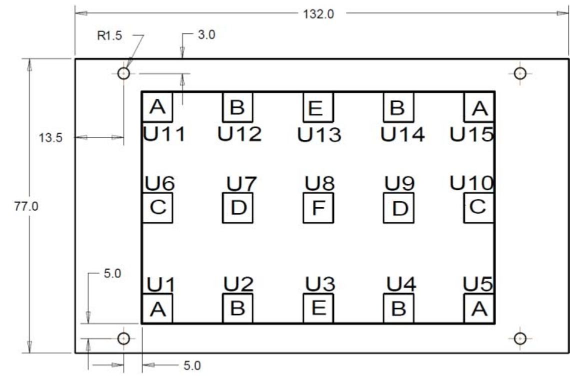

Fig. 1. JESD22-B111 drop test board outline and component locations.

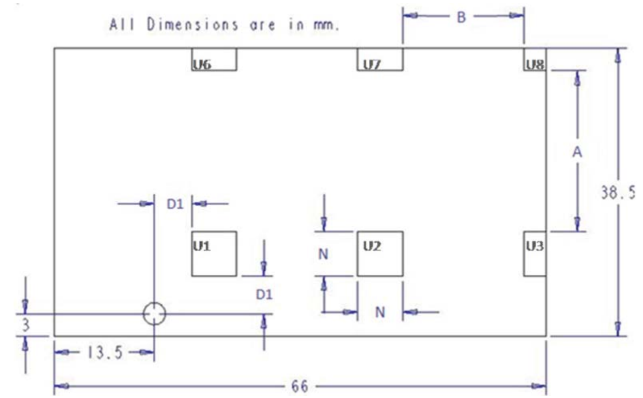

Fig. 2. Dimension parameters for a quarter part of the modified JEDEC board.

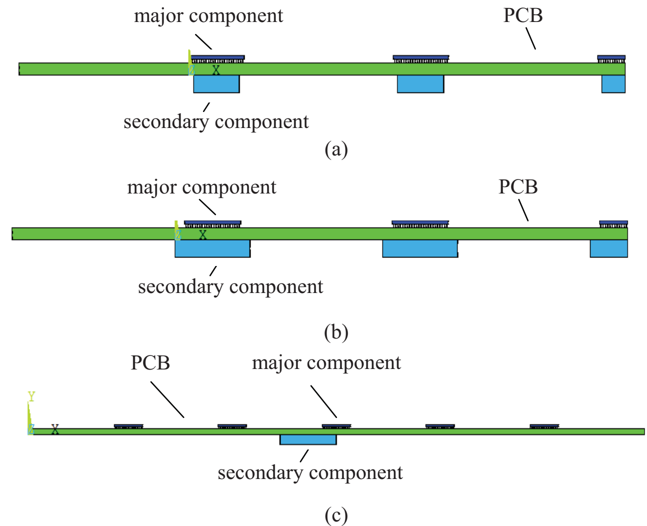

Fig. 3. Three scenarios of the secondary component attachment. (a) Secondary component is smaller than the major component. (b) Secondary component is larger than the major component. (c) Larger secondary component is placed off-center relative to the major component.

C. Drop Orientations

JESD22-B111 standard uses horizontal drop with components face-down (0°) as the testing condition, as shown

in Fig. 4(a). In real-life drops, system board may experience different impact orientations. In this paper, components face-up in a horizontal drop (180° rotation) [Fig. 4(b)], and a vertical drop (90° rotation) [Fig. 4(c)], are studied.

III. Finite Element Models

The details of finite element analysis are referred to the previous papers [7]–[10], [16], [17], [23]. Global and local finite element modeling techniques are applied in this paper. In the global finite element model, the symmetry conditions are applied whenever it is possible to reduce the problem size. A local finite element model is developed at any desired location of the components on the board. Under impact loading, the corner solder balls in a component are usually most vulnerable to crack. Therefore, those solder ball(s) in the local model are created with all necessary information and the refined meshes. Since the primary failure is at the intermetallic layer of solder balls [2], a fixed thickness layer of elements is used at the critical solder ball upper interface to capture the stresses at interface throughout all simulations. Linear elastic implicit dynamic analysis is applied in this paper.

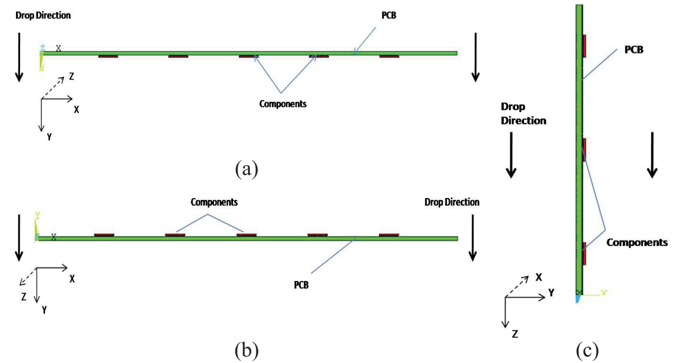

Fig. 4. Drop orientations. (a) Horizontal drop with components face-down (0°). (b) Horizontal drop with components face-up (180°). (c) Vertical drop (90°).

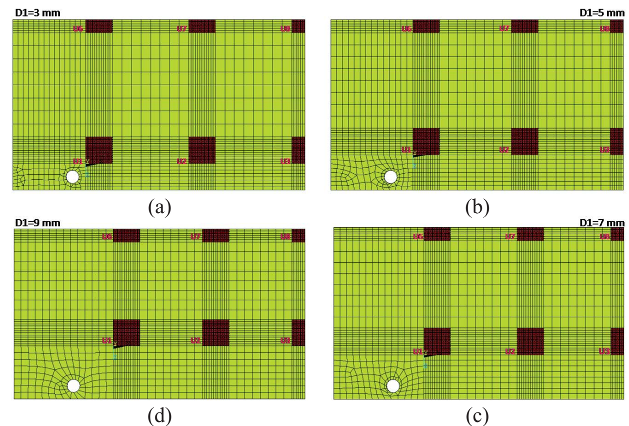

Fig. 5. Global finite element models of the quarter test board with varying distance $D1$ ($D1$ as denoted in Fig. 2). (a) $D_1 = 3$ mm. (b) $D_1 = 5$ mm. (c) $D_1 = 7$ mm. (d) $D_1 = 9$ mm.

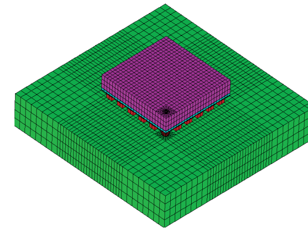

Fig. 6. Local finite element model with refined meshes for the critical solder ball.

IV. Results

A. Effects of Major Component Locations

Fig. 5 shows the global finite element models of the quarter board assembly, with varying distances $D1$ of 3–9 mm (from the edge of corner component to the mounting hole with respect to x- and y-directions), respectively. As $D1$ increases, the components on the board move away from screw mount and are "squeezed" toward the center of board.

Fig. 6 shows the local finite element model with refined meshes for a corner ball: the outer most corner on the right side, which is expected to be most critical. The local model can be at any locations, for example, at U1 or U8 positions.

Fig. 7(a) plots the peeling stress history of the critical solder ball in the corner component U1 for 12 × 12 array packages (0.5-mm pitch, 6 mm × 6 mm package size). It clearly shows that the distance $D1$ has a significant impact on the solder ball stress, which monotonically decreases with the increase of $D1$. The closer the component U1 is placed to the screw hole, the higher the stress is. Fig. 7(b) shows the peeling stress history of the critical solder ball in the center component U8. Four curves almost coincide with each other. This implies that the ball stress in U8 stays almost the same regardless of $D1$. This is probably due to two reasons: 1) the distance from U8 to mounting hole does not change when $D1$ varies and 2) component U8 is so far away from the mounting hole that the mounting constraint has a negligible effect on the center component.

Fig. 8 plots the maximum peeling stresses with different $D1$ for a package size of 3 mm × 3 mm, 6 mm × 6 mm, and 10 mm × 10 mm, respectively. For these three WLP sizes, the maximum peeling stress at U1 is very sensitive to the distance $D1$, and the stress decreases exponentially with the increased distance. As expected, the maximum peeling stress in U8 stays approximately the same regardless of $D1$ for each package size. From those figures, it is observed that beyond certain distance, the stress in U1 is lower than that in U8, suggesting that the center component may fail before the corner component. As mentioned previously, JEDEC standard specifies a 5-mm distance between the corner component and the nearest mounting screw. For small-size WLPs [3 mm × 3 mm and 6 mm × 6 mm in Fig. 8(a) and (b)], stress in U1 is higher than U8, but the results are opposite for large-size WLPs [10 mm × 10 mm in Fig. 8(c)]. Experimental data have verified the shift of failures from U1 to U8 when package size increases [2]. Fig. 8 suggests that a 6-mm distance seems to be the crossover point for all package sizes. Beyond 6 mm, the stress caused by mounting constraints on the corner components will be less significant.

Further, Fig. 9 plots the PCB board x-component strain at the corners of U1 and U8, respectively. It shows that

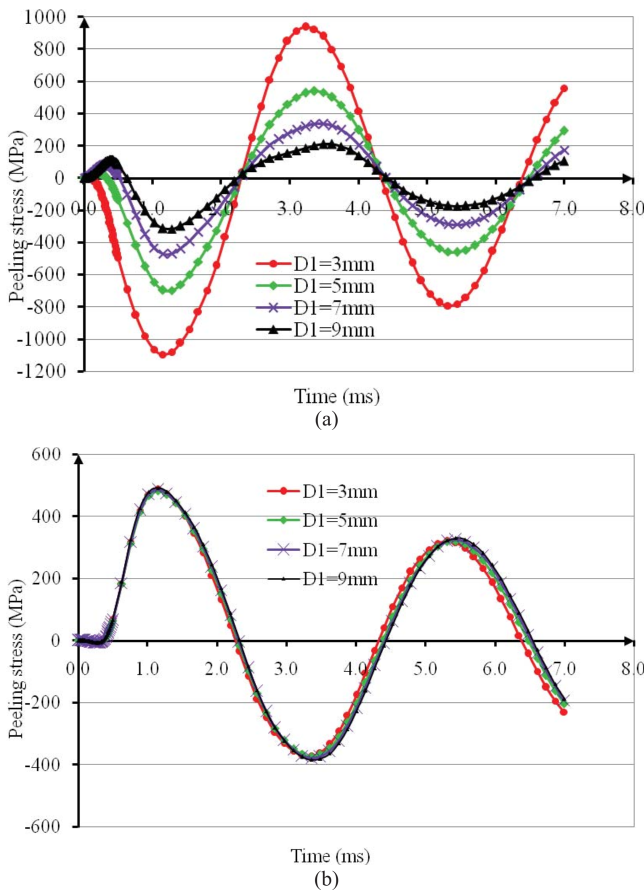

Fig. 7. Peeling stress of the critical solder ball with varying $D1$. (a) Component U1. (b) Component U8.

the bending at U1 is in a reversed mode compared to the bend direction at U8. The localized PCB bend mode near the mounting hole causes excessive stresses in solder balls if the component is not far enough away from it. Fig. 9 shows that with $D1 = 5$ mm, the bending strain of the board at U1 is greater than U8. This has also been validated by experimental data [2].

These results suggest: 1) excessive stresses appear in the solder balls for the components placed near the mounting screws, and the closer the component is placed, the greater the stress is; 2) board bend near the mounting hole is in an opposite direction compared to the PCB bend at the center; 3) in a real system board design, the components should be placed far enough away from the mounting holes wherever possible, and it is recommended that 6 mm of the distance may be a reference value; and 4) the solder ball stress always increases with package size for the components placed in the center of the board.

B. Effects of Secondary Components

Finite element analysis is conducted to investigate the effects of the secondary components attachment. The JEDEC drop test board design without any secondary component placement is used as the baseline model. Fig. 10 shows the detailed information of the local finite element models for scenarios 1 and 2, as defined previously in Fig. 3. In this paper, 12 × 12 array WLP (6 mm × 6 mm) are used as major components. Since the primary interest of this paper is the solder ball stress/strain of major components, the secondary component is simplified as a block with an effective modulus and mass density, as shown in Fig. 10.

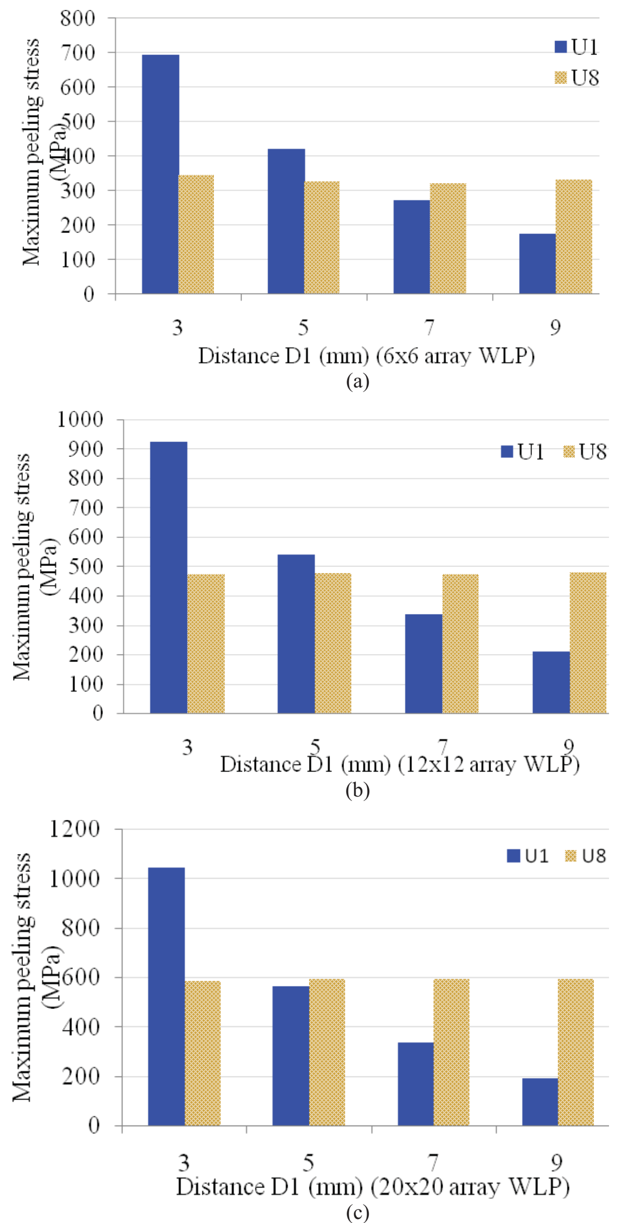

Fig. 8. Maximum peeling stresses in U1 and U8. (a) 6 × 6 array. (b) 12 × 12 array. (c) 20 × 20 array packages, with varying D_1.

Fig. 11 shows the results of finite element simulations for scenarios 1 and 2, compared to the results without secondary component placement. It is interesting to see that when the secondary component is smaller than the major one, the peeling stress of critical solder balls is reduced only slightly. The drop life in this case is expected to stay approximately same or slightly better than in the reference case where there is no secondary component. However, when the size of the secondary component is greater, the solder ball peeling stress is significantly reduced for both U1 and U8. This means,

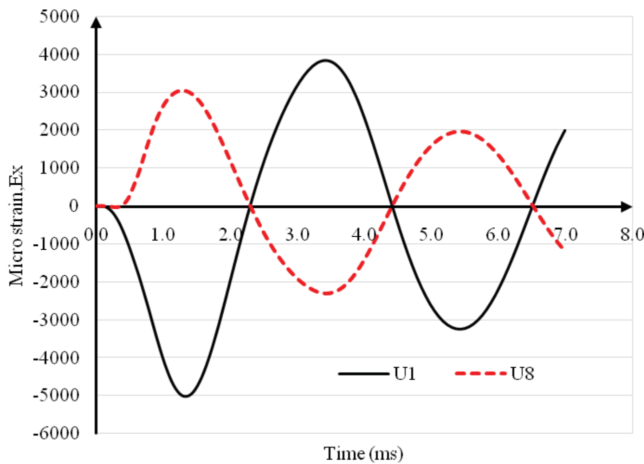

Fig. 9. Board strain component in x-direction in U1 and U8 (12 × 12 array package, $D1 = 5$ mm).

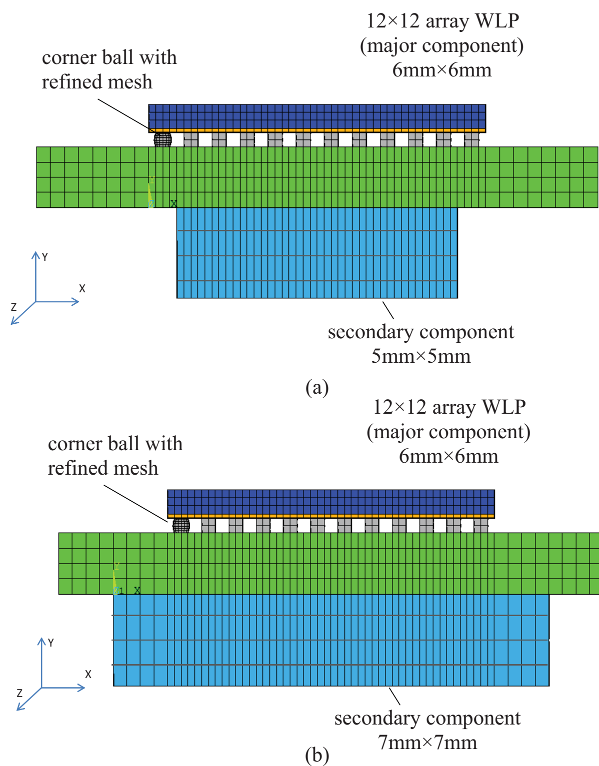

Fig. 10. Local finite element models of scenarios 1 and 2. (a) Secondary component is smaller than the major one. (b) Secondary component is larger than the major one.

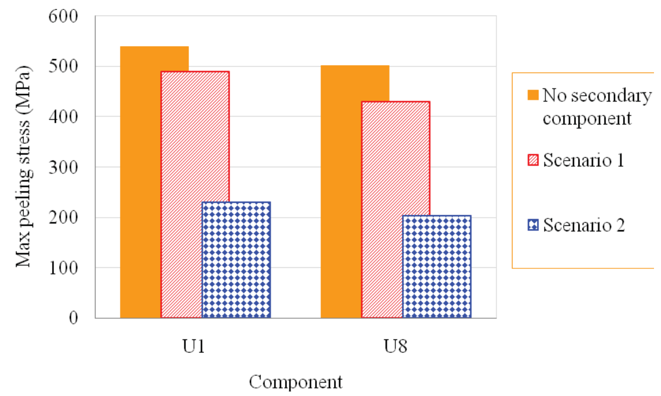

Fig. 11. Comparisons of peak peeling stresses at components U1 and U8 for scenarios 1 and 2.

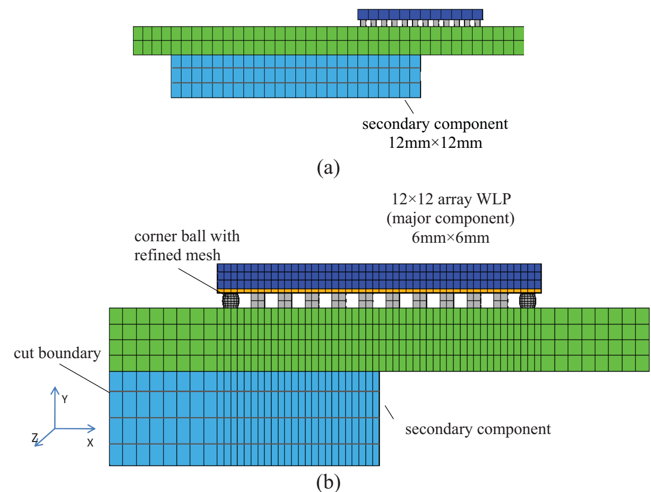

Fig. 12. Finite element model detail for scenario 3. (a) Zoomed-in global finite element model. (b) Local finite element model.

the drop performance can be greatly improved. For a smaller secondary component attachment, it does not affect board bending outside the major component, therefore the solder ball stresses are reduced only slightly. However, for a larger secondary component, board strain in the proximity of corner balls of major components is reduced significantly due to local stiffening. This suggests that a larger component mounted and aligned in the center beneath the major component in system board is beneficial to the solder ball drop performance.

Now let us consider scenario 3 when the secondary component is mounted off-center with respect to the major component. Fig. 12(a) shows a zoomed-in front view of the global finite element model for the size and position of the secondary component in scenario 3, defined in Fig. 3(c). Again 12 × 12 array wafer-level packages (6 mm × 6 mm) are used as major components, and the secondary components of 12 mm × 12 mm are placed beneath the central columns of U3, U8, and U11, with partial overlap. Fig. 12(b) is the detail of the local finite element model, in which both corner balls are made with refined meshes due to the nonsymmetry.

Fig. 13 shows the contour plot of peeling stress in all solder balls for U8 in scenario 3. The baseline model results are also included in this figure for comparison. It shows that the stresses in solder balls on the left corner are considerably reduced due to the presence of secondary component. However, on the right side, solder ball stresses are greater than the baseline model results. Fig. 14 further shows the maximum peeling stresses of the left corner ball, right corner ball, and baseline model results. The increase of stress on the right-hand side in solder balls is probably due to the local bending enhancement by the secondary component. This may be viewed as some constraints placed on U8 to give rise to excessive stresses on the right, which is similar to the effect of the mounting hole.

Fig. 15 shows the solder ball crack maps from an experiment of a test board with a large BGA mounting offset from

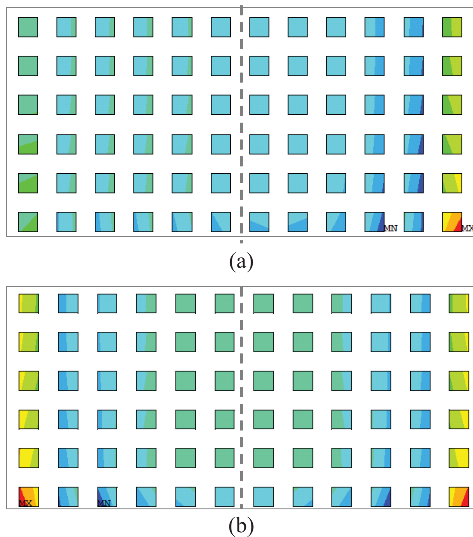

Fig. 13. Contour plots of solder balls of U8 (only half are shown) (a) with a large secondary component placement in scenario 3 and (b) baseline model without secondary components.

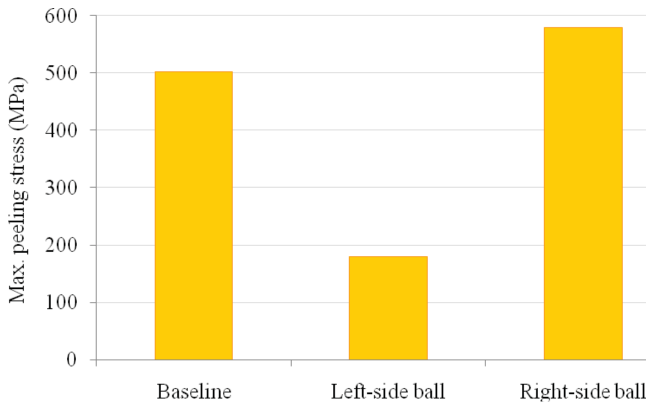

Fig. 14. Maximum peeling stresses for scenario 3 (local model results).

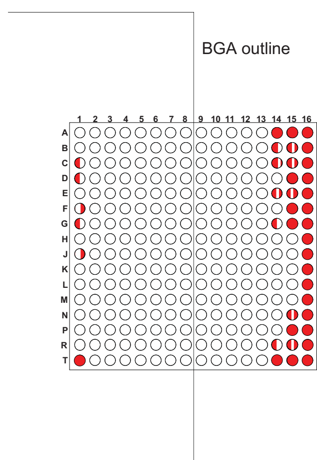

Fig. 15. Solder ball crack map for U8 in scenario 3.

WLP (scenario 3). There is more damage on solder balls next to WLP right edge, which is away from the BGA mount. Experimental results are well aligned with finite element analysis presented above.

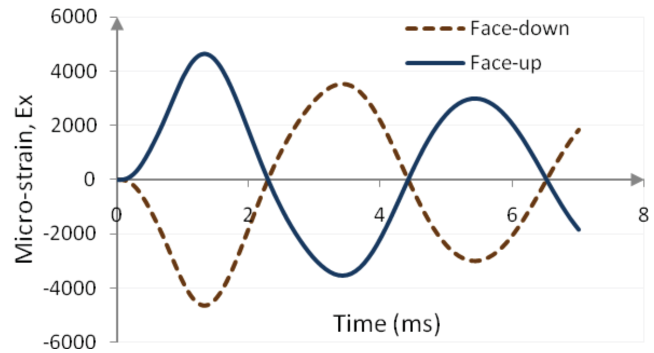

Fig. 16. Board strain x-component at U1.

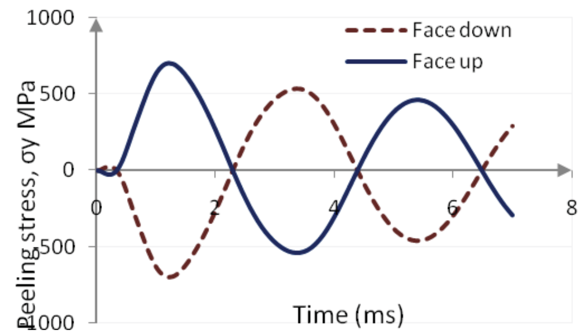

Fig. 17. Peeling stress history at U1.

C. Effects of Drop Orientations

1) Component Face-Down (0°) Versus Face-Up (180°) Drop Orientations: JESD22-B111 standard uses component face-down as a test condition, which refers to the board side with components in the direction of drop, as shown in Fig. 4(a). It is of interest to understand the difference due to a different component orientation. Experiments have observed that the failure rate for center component (Group F) is higher in face-down drop. However, corner Group A fails much earlier in face-up drop [2]. This implies that drop test reliability varies with component orientation. To explain the difference, finite element analysis with JEDEC test board for 12 $\times$ 12 array WLPs is performed. Fig. 16 plots the strains in x-direction at components U1 for both face-down and face-up drops. Since the same point (1 mm $\times$ 1 mm away from component U1 edge on the board side with components) is used in calculating board strain, Fig. 16 shows exactly the "mirrored" results for board strain due to the symmetry of loading for 0° versus 180° drop. The peeling stresses in solder ball also show the similar pattern, as in Fig. 17.

Solder ball fracture during horizontal drop is dominantly caused by peeling stress (tensile stress) due to PCB bending. From the above results, it can be seen that tensile stress in 0° drop becomes compressive in 180° drop, and verse visa. Fig. 18 shows the maximum peeling stress in U8 and U1 on JEDEC drop test board for face-up versus face-down drop. It shows that the maximum tensile stress at U1 is greater in face-up drop, while the maximum tensile stress at U8 is greater in face-down drop. These data explained the experimental observations well.

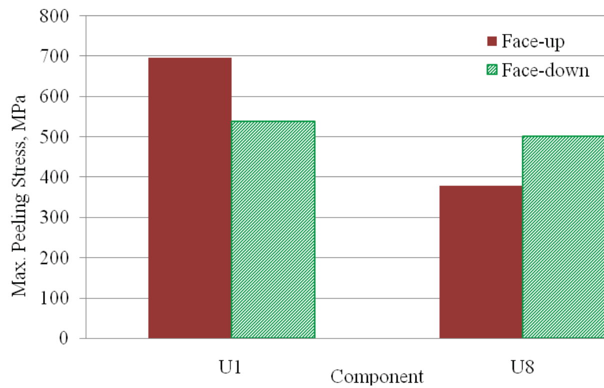

Fig. 18. Maximum tensile stresses in U1 and U8 on JEDEC drop test board.

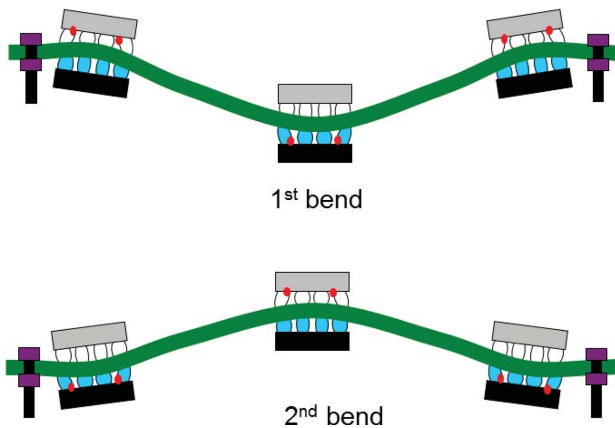

Fig. 19. Illustration of solder ball damages for component face-down and face-up configurations.

Solder balls experience tensile stress when the board bends away from the component. For component face-down drop, the critical solder balls experience tensile stress when the board has positive curvature. On the other hand, for component face-up drop, the critical solder balls experience tensile stress when the board has negative curvature. The board bending during drop is illustrated in Fig. 19. Corner and center components are depicted in the figure for both component face-down (dark color) and face-up (light color) drops. The board bends downward first (first peak bend), and then upward (second peak bend) in the first period. During the first peak bend mode, the board has positive curvature in the middle and negative curvature near mounting holes, and it is opposite at the second peak bend mode. The vibration attenuates afterward. For component face-down drop, the center component experiences tensile stress at the first bend when the board center has negative curvature. The corner component experiences peeling force and cracks initiate at the second bend when the board near mounting screws has negative curvature. For the component face-up drop orientation, on the other hand, the solder ball crack initiates at the second bend for center component, and at first bend for corner component. Since the board bending magnitude is greater at the first bend than the second bend, the corner component solder joints see higher maximum peeling stress in the face-up orientation. Therefore, the corner components fail faster in face-up drop.

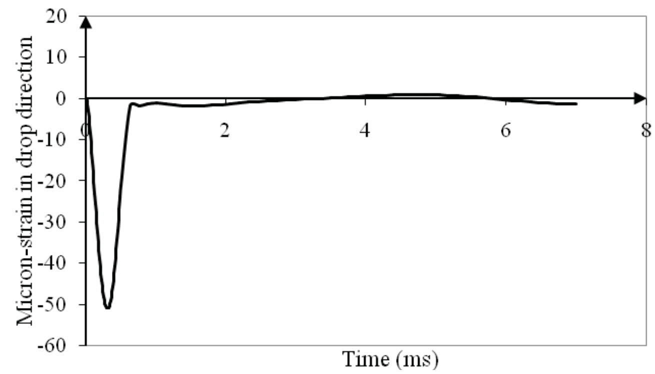

Fig. 20. Board strain in drop direction at U8.

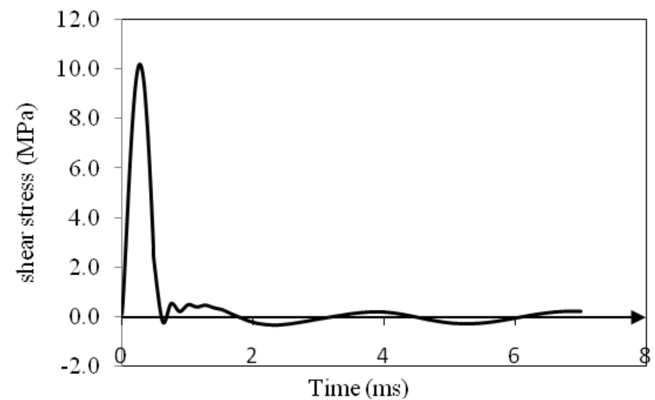

Fig. 21. Shear stress at U8.

2) Vertical Drop (90°) Orientation: During a horizontal drop (either 0° or 180° drop), the impact energy is converted to the strain energy of the board assembly in the form of bend, as illustrated in Fig. 19. Board bend induces the stresses in solder balls. Wong *et al.* [24], [25] studied an extreme case when the board is rigid enough, and found that stresses in solder balls are insignificant. Now let us turn our attention to a vertical drop, as defined in Fig. 4(c). It should be noted that in this configuration, the impact energy is mainly converted to the strain energy of the board assembly in the form of compression or extension in vertical direction. Since the components on the board are rather small and light compared to the board, board bending due to component mass is almost negligible. It is expected that shear stress becomes dominant in causing solder ball failures. Fig. 20 plots the strain component of the board in drop direction near component U1. It can be seen that the magnitude of the strain is three orders less than the board strain in a horizontal drop. Fig. 21 plots the shear stress in the critical solder ball at U1, in which the peeling stress (or normal stress to the board plane) is not shown, since the peeling stress is an order lower than the shear stress. Even the magnitude of the shear stress in this figure is much less than that in a horizontal drop. This implies that a very limited damage can be induced during a vertical drop for solder balls. Chong *et al.* [5] conducted an experiment for vertical drop based on JEDEC drop test board. No solder ball failures were observed after 150 drops.

These results suggest that: 1) 0° or 180° drop may be the worst drop orientation for solder ball damages. In this

configuration, excessive board bending is induced to cause significant stresses (in tensile form) in the solder balls; 2) package performs differently for 0° versus 180° drop, since the magnitude of tensile and compressive stresses in one vibrational period is not symmetric and location dependent; and 3) the vertical drop generates very limited damage to the solder balls. The impact energy in a vertical drop is converted to the strain energy of board in in-plane compression and extension. Such deformation is very limited compared to board flexing. In a vertical drop, shear stress is dominant to cause solder ball failures, but the magnitude of the shear stress is orders less than that in a horizontal drop.

V. Conclusion

The placement of major components, the effect of secondary components attachment, and the drop orientations were studied in this paper to investigate the component behavior at board and system level under impact loading. Near the mounting screws region, there exists a reversed board bend mode with respect to the bend mode in the center. This localized bend mode causes excessive stresses in solder balls for the components close to the mounting screws. It is recommended that the components are placed far enough (e.g., 6 mm based on JEDEC test board dimension) to avoid high stresses. The attachment of a secondary component beneath a major component has different effects on major component reliability: symmetric mounting can reduce the stresses in the major component, in particular, when the size of the secondary component is greater. However, the off-centered mounting gives rise to the additional stresses in solder balls on the far edge of the major component, and therefore can lead to higher failure rates. Components respond differently under 0° (face-down) and 180°(face-up) horizontal drops, since the magnitude of tensile and compressive stresses in one vibrational period is not symmetric. In addition, horizontal drop may be the worst drop orientation for solder ball damages, compared to the other drop orientations. The vertical (90°) drop has very limited damages to solder balls. The findings and predictions were verified experimentally. The results provide insight to the system and board-level designs in product development.

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References

[1] *Board Level Drop Test Method of Components for Handheld Electronic Products*, JEDEC Standard JESD22-B111, 2003.

[2] T. Zhou, R. Derk, K. Rahim, and X. J. Fan, "Larger array finepitch wafer level package drop test reliability," in *Proc. ASME Conf. Collocat. Summer Heat Transf. Conf. Int. Energy Sustain.*, 2009, pp. 689–701.

[3] T. Y. Tee, J. E. Luan, E. Pek, C. T. Lim, and Z. W. Zhong, "Advanced experimental and simulation techniques for analysis of dynamic responses during drop impact," in *Proc. 54th Electron. Compon. Technol. Conf.*, 2004, pp. 1089–1094.

[4] T. Y. Tee, T. B. Tan, R. Anderson, H. S. Ng, J. H. Low, C. P. Khoo, R. Moody, and B. Rogers, "Advanced analysis of WLCSP copper interconnect reliability under board level drop test," in *Proc. Electron. Packag. Technol. Conf.*, 2008, pp. 1086–1095.

[5] D. Y. R. Chang, H. J. Toh, B. K. Lim, and P. T. H. Low, "Drop reliability performance for PCB assemblies of chip scale packages (CSP)," in *Proc. Electron. Packag. Technol. Conf.*, 2005, pp. 262–269.

[6] A. Syed, M. S. Kim, W. Lin, Y. J. Khim, S. E. Song, H. J. Shin, and T. Panczak, "A methodology for drop performance prediction and application for design optimization of chip scale packages," in *Proc. Electron. Compon. Technol. Conf.*, 2005, pp. 472–479.

[7] H. S. Dhiman, X. J. Fan, and T. Zhou, "Modeling techniques for board level drop test for a wafer-level package," in *Proc. Int. Conf. Electron. Packag. Technol. High Density Packag.*, Jul. 2008, pp. 1–9.

[8] H. S. Dhiman, X. J. Fan, and T. Zhou, "JEDEC board drop test simulation for wafer level packages (WLPs)," in *Proc. Electron. Compon. Technol. Conf.*, 2009, pp. 556–564.

[9] A. S. Ranouta and X. J. Fan, "Investigations of solder ball drop reliability: BGA versus WLP," in *Proc. Int. Conf. Electron. Packag. Technol. High Density Packag.*, 2011, pp. 1–6.

[10] X. J. Fan, A. S. Ranouta, and H. S. Dhiman, "Effect of structure and material at package level on solder joint reliability under impact loading," *IEEE Trans. Comp., Packag. Manuf. Technol.*, 2012, to be published.

[11] Z. J. Xu and T. X. Yu, "Board level dynamic response and solder ball joint reliability analysis under drop impact test with various impact orientations," in *Proc. Electron. Packag. Technol. Conf.*, 2008, pp. 1080–1085.

[12] J. Luan and T. Y. Tee, "Novel board level drop test simulation using implicit transient analysis with input-G method," in *Proc. 6th Electron. Packag. Technol. Conf.*, 2004, pp. 671–677.

[13] S. Irving and Y. Liu, "Free drop test simulation for portable IC package by implicit transient dynamics FEM," in *Proc. 54th Electron. Compon. Technol. Conf.*, 2004, pp. 1062–1066.

[14] W. K. Loh, L. Y. Hsiang, and A. Munigayah, "Nonlinear dynamic behavior of thin PCB board for solder joint reliability study under shock loading," in *Proc. Int. Symp. Electron. Mater. Packag.*, 2005, pp. 268–274.

[15] L. X. Shen, "Simulation of drop test board with 15 components using explicit and implicit solvers," presented at the Int. ANSYS Conf., 2008.

[16] H. S. Dhiman, "Study on finite element modeling of dynamic behaviors of wafer level packages under impact loading," M.S. thesis, Dept. Elect. Mech. Eng., Lamar Univ., Beaumont, Texas, 2008.

[17] A. S. Ranouta, "Effects of orientation, layout, component structure and geometry on drop reliability of chip scale packages (CSPS)," M.S. thesis, Dept. Elect. Eng. Mech. Eng. Packag., Lamar Univ., Beaumont, Texas, 2010.

[18] W. Ren and J. Wang, "Shell-based simplified electronic package model development and its application for reliability analysis," in *Proc. Electron. Packag. Technol. Conf.*, 2003, pp. 217–222.

[19] W. Ren, J. Wang, and T. Reinikainen, "Application of ABAQUS/explicit submodeling technique in drop simulation of system assembly," in *Proc. Electron. Packag. Technol. Conf.*, 2004, pp. 541–546.

[20] L. Zhu, "Modeling technique for reliability assessment of portable electronic product subjected to drop impact loads," in *Proc. 53rd Electron. Compon. Technol. Conf.*, 2003, pp. 100–104.

[21] P. Lall, D. Panchagade, D. Iyengar, S. Shantaram, J. Suhling, and H. Schrier, "High speed digital image correlation for transient-shock reliability of rlectronics," in *Proc. 57th Electron. Compon. Technol. Conf.*, 2007, pp. 924–939.

[22] P. Lall, S. Gupte, P. Choudhary, and J. Suhling, "Solder-joint reliability in electronics under shock and vibration using explicit finite-element sub-modeling," in *Proc. 56th Electron. Compon. Technol. Conf.*, 2006, pp. 428–435.

[23] X. J. Fan, B. Varia, and Q. Han, "Design and optimization of thermo-mechanical reliability in wafer level packaging," *Microelectron. Reliab.*, vol. 50, no. 4, pp. 536–546, 2010.

[24] E. H. Wong, Y.-W. Mai, and S. K. W. Seah, "Board level drop impact-fundamental and parametric analysis," *Trans. ASME J. Electron. Packag.*, vol. 127, pp. 496–502, 2005.

[25] E. H. Wong, C. T. Lim, J. E. Field, V. B. C. Tan, V. P. M. Shim, K. T. Lim, and S. K. W. Seah, "Tackling the drop impact reliability of electronic packaging," in *Proc. ASME Int. Electron. Packag. Tech. Conf.*, Jul. 2003, pp. 1–9.

Xuejun Fan received the Ph.D. degree from Tsinghua University, Beijing, China, in 1989, and the Bachelors and Masters degrees from Tianjin University, Tianjin, China, in 1984 and 1986, respectively.

He is an Associate Professor with the Department of Mechanical Engineering, Lamar University, Beaumont, TX. He was a Senior Staff Engineer with Intel Cooperation, Chandler, AZ, from 2004 to 2007, a Senior Research Member with Philips Research Laboratory, Briarcliff Manor, NY, from 2001 to 2004, and a Technical Staff Member and the Group Leader with the Institute of Microelectronics, Singapore, from 1997 to 2000. He was promoted to a Full Professor with the Taiyuan University of Technology, Shanxi, China, in 1991, and became one of the youngest full professors in China at that time. He has authored or co-authored more than 130 technical papers and three books entitled *Mechanics of Microelectronics, Moisture Sensitivity of Plastic Packages of IC Devices*, and *Solid State Lighting Reliability: Components to System*. He holds five patents. His current research interests include design, modeling, material characterization, and reliability in micro- and nanoelectronic packaging and microsystems.

Dr. Fan was a recipient of the IEEE CPMT Exceptional Technical Achievement Award in 2011, and the Best Paper Award of the IEEE TRANSACTIONS ON COMPONENTS AND PACKAGING TECHNOLOGIES in 2009. He is an IEEE CPMT Distinguished Lecturer. He was a nominee for the Ten Outstanding Youth of China Award in 1991.

Amarinder Singh Ranouta received the B.S. and M.S. degrees in mechanical engineering from Punjab Technical University, India, and Lamar University, Beaumont, TX, respectively.

He has authored or co-authored several papers in journals and conferences, on finite element modeling of the dynamic behaviors of semiconductor packages.

Mr. Ranouta was a recipient of the Lamar University Graduate Studies Scholarship.